

HIGH SPEED TxDAC's

DDS/Current Output: D/A's																	
				Power Supply			Output				Settling	Glich	Up			Model Designator	
				Requirements			Current	INL	DNL	Time	Im	Date	THD	SFDR	Temperature		
	#	#	Interpo	+Vcc	+Icc	Isleep	mA				pulse	Rate			Range	#	Price
MODEL	Bits	D/A's	Factor	+ Volts	+ mA	+ mA	min	Lsb	Lsb	nsec	pV-sec	Max	-dBc	dBc	-40 85	-55 125	of Pins /100's
AD9708	8	1		+3/5V	35/28	8	2>20	1/2	1/2	35	5	100	67 @Fout=1Mhz, fclk=10Mhz	50 @Fout=1Mhz, fclk=10Mhz	A		28 \$6.00
AD9760-50	10	1		+5V	35	8	20	1	1/2	35	5	50	70 @Fout=1Mhz, fclk=50Mhz	68 @Fout=1Mhz, fclk=50Mhz	A		28 \$8.50
AD9760	10	1		+5V	35	8	20	1	1/2	35	5	100	73 @Fout=1Mhz, fclk=50Mhz	70 @Fout=1Mhz, fclk=50Mhz	A		28 \$10.00
AD9762	12	1		+5V	30	8.5	20	2 1/2	1 1/2	35	5	100	74 @Fout=1Mhz, fclk=25Mhz	75 @Fout=1Mhz, fclk=25Mhz	A		28 \$17.86
AD6742	12	1				NA			3/4	5	1.5	65		78 @Fout=19.5Mhz , fclk=64Mhz	A		28
AD9764	14	1		±5V +5V	±100 25	8.5	±0.5V 20	1 4	2	35	NS	100	75 @Fout=5Mhz, fclk=100Mhz	84 @Fout=5Mhz, fclk=100Mhz	A		28 \$33.26
AD9761	10	2	2X	+2.7/5V	70/120		10	1 3/4	1 1/4	35	5	40	58 @Fout=10Mhz, fclk=40Mhz	59 @Fout=1Mhz, fclk=40Mhz	A		28 \$13.95
AD9774	12	1	4X	+5V			20	2 1/2	1 1/2	35	5	32	76 @Fout=1.01Mh z, fclk=25Mhz	77 @Fout=5Mhz, fclk=25Mhz	A		28 \$40.00
AD9778	12	1	8X	+5V								32			A		28